(Please write your Exam Roll No.) *Exam Roll No. .....*

END TERM EXAMINATION

SECOND SEMESTER [BCA] MAY JUNE 2017

Paper Code: BCA-106 ***Subject: Digital Electronics (Batch 2011 onwards)***

Time: 3 Hours ***Maximum Marks: 75***

Note: Attempt any five questions including Q.no.1 which is compulsory. Select one question from each unit.

Q1 Attempt **any five** from the following:- **(5x5=25)**

(a) Design full subtractor circuit using NAND gate only.
(b) Explain how transistor as a switch works? Give its use in logic circuits.
(c) Define fan-in, fan-out, propagation delay, noise margin and voltage parameters.
(d) Explain decoder and demultiplexer. Give their applications.
(e) State the De Morgan's theorem and prove them with an example.
(f) Define synchronous and asynchronous counters with their merit and demerits.

UNIT-I

Q2 Simply the expressions:-

(a) $AB + \overline{AC} + A\bar{B}C(AB + C)$ **(3)**
(b) Explain the operation and advantages of CMOS. **(6.5)**
(c) Prove $A + \bar{A}B = A + B$ **(3)**

Q3 (a) Design a combinational circuit whose input is three bit number and whose output is equal to square of input and implement it using basic gates. **(6.5)**
(b) Explain briefly the BCD to seven segment decoder. **(6)**

UNIT-II

Q4 (a) Design a full adder circuit using Multiplexer. **(6.5)**
(b) Implement the Ex-OR gate equation with NAND gates only. **(6)**

Q5 (a) Draw the logic diagram of parity checker and generator/checker. Explain its operation with the help of truth table. **(6.5)**
(b) Design a binary multiplier for following: A=1011, B=111 **(6)**

UNIT-III

Q6 (a) Define edge triggering in flip-flops. Explain Master slave JK flip-flop that solves the problem of Race-around condition, with diagram. **(7)**
(b) Design JK flip-flop using SR flip-flop. **(5.5)**

Q7 (a) Explain the bidirectional shift register with diagram, truth table and clock pulse. Give their applications. **(7.5)**
(b) Differentiate Static RAM and Dynamic RAM. **(5)**

UNIT-IV

Q8 (a) Design Modulo 7 counters with truth table and logic diagram. **(7.5)**
(b) Give the application of PLA and PLD. **(5)**

Q9 (a) Design a combinational circuit with PLA, having three inputs, four product terms and two outputs: **(7.5)**
F1(A,B,C)=Σ(3,5,6,7), F2(A,B,C)=Σ(0,2,4,7)
(b) Explain Johnson's counter with truth table and clock pulses. **(5)**

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